REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the final Office Action of October 28, 2008 (hereinafter "Final Action") and the Advisory Action dated January 7, 2009 (hereinafter "Advisory Action"). In response, Applicants have amended independent Claims 1, 10, 11, and 21 as indicated above to clarify the recitations thereof. In particular, Claims 1, 10, 11, 21 and the claims dependent therefrom have been amended to recite memory cell "regions" therein, while Claims 1, 10, 11, and 21 have been amended to clarify that "n is an integer equal or greater than 2," and "m is an integer equal or greater than 4", as suggested by the Examiner in the "Response to Arguments" section of the Final Action. *See* Final Action, Page 2. Support for these amendments can be found, for example, in Figure 3 of the present specification. No new matter has been added.

Accordingly, Applicants respectfully request reconsideration of the pending claims for the reasons discussed below.

The Section 112 Rejections

Claims 1, 10, 11, and 21 stand rejected under 35 USC §112, second paragraph, as being indefinite. *See* Final Action, Pages 2-3. In particular, the Final Action asserts that these Claims are rejected because "[t]he claims identify 'nm' as the number of memory cell arrays, and then the same 'n' and 'm' are being identified as the number of word lines and column lines respectively." Final Action, Page 3. The Final Action further asserts that there is insufficient antecedent basis for the recitations of "y" in Claims 1, 10, 11, and 21.

In response, Applicants respectfully note that Claim 1 recites "*n* word lines" and "*m* column selecting signal lines." Claim 1 further recites that "*nm* comprises *n* multiplied by *m*." Thus, Claim 1 clearly points out that, if the number of word lines is *n* and the number of column selecting signal lines is *m*, then the number of memory cell regions is *nm* (e.g., *n* multiplied by *m*).

Applicants also submit that the recitations of "*y*" do not appear to present any antecedent basis issues. Indeed, as noted in the MPEP, "[t]he mere fact that the body of a

claim recites additional elements which do not appear in the claim's preamble does not render the claim indefinite under 35 U.S.C. 112, second paragraph." MPEP, §2173.05(e). Applicants further note that amended Claim 1 recites that "*y*" is an integer "greater than 1" but "less than *nm*."

Thus, Applicants respectfully submit that the recitations of Claim 1 particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, Applicants respectfully request withdrawal of the rejections under 35 USC §112, second paragraph for at least these reasons.

Independent Claims 1, 10, 11, and 21 Are Patentable Over the AAPA and Kim

Independent Claims 1, 10, 11, and 21 stand rejected under 35 U.S.C. §103(a) as obvious over the alleged "Applicants' Admitted Prior Art" (AAPA[1]) in view of U.S. Patent No. 7,013,413 to Kim et al. (hereinafter "Kim"). Claim 1, as amended, recites:

> 1. A method for testing a semiconductor memory device including nm memory cell regions for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected, and each half of the nm memory cell regions is a first memory cell array and a second memory cell array, the method comprising:
>
> extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell regions in a test data write step; and
>
> comparing the x-bit data output from each of the nm memory cell regions to generate nm-bit comparison result data, and **sequentially outputting y-bit comparison result data selected by selecting, by y bits generated from the first memory cell array or from the second memory cell array, the nm-bit comparison result data** in response to a control signal **to the y data I/O pads**, respectively, in a test data read step,
>
> **wherein n is an integer equal or greater than 2, wherein m is an integer equal or greater than 4, wherein x and y are integers greater than 1**, wherein nm comprises n multiplied by m, and **wherein y is less than nm**. (*Emphasis added*).

Applicants respectfully submit that the combination of the AAPA and Kim fails to

1 For convenience, Applicants have adopted the term "Applicants' Admitted Prior Art (AAPA)" used in the Office Action. Use of this term is not an admission by Applicants that the material cited in the Office Action is prior art.

disclose or suggest at least the recitations of amended Claim 1 highlighted above. For example, the Final Action concedes that the AAPA fails to disclose or suggest sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data, but argues that Kim provides these recitations. *See* Final Action, Page 4.

Applicants respectfully disagree. As provided by a cited portion of Kim:

> Referring to **FIG. 4**, in a memory device according to an embodiment of the present invention, the read data comparing part **500** comprises a number of comparators **501-508** for receiving 8 bits data RD<0:7> read from the core cell region **100** according to a control signal (S_DATEST) when it is a DA mode test, compressing upper 4-bit data RD<0:3> and a lower 4-bit data RD<4:7> and generating a 1-bit data error<i>, 0<i<7, having information indicating whether a failure exists, multiplexers **509-512** for selecting the 8-bit data RD<0:7> read from the core cell region **100** when it is a normal mode or error <0:7> generated by the comparators **501-508** when it is a DA mode test according to the control signal (S_DATEST).

Kim, Col. 4, lines 55-67 (*emphasis added*). Accordingly, Kim discloses a circuit including comparators **501** to **508** that compare write data WD and read data RD to generate error signals error<0> to error<7>, respectively. As further illustrated in Figure 4 of Kim, the multiplexers **509-512** select between the 8-bit read data RD<0:7> (in normal mode) and the 8-bit error data error<0:7>(in test mode) for output in response to the control signal S_DATEST. *See* Kim, Fig. 4.

However, as shown in Figure 4, Kim discloses that all of the error data error<0:7> is output to the pad DQB0 via the shift register **301**. In particular, Kim describes that "[t]he selected parallel data is forwarded to the shift register **301**...and further converted into serial data via the multiplexer and driver **401**...and outputted via a corresponding output pad DQB0." Kim, Col. 6, lines 8-13. Accordingly, while Kim may disclose serially outputting the 8-bit data error<0:7>, nowhere do the cited portions of Kim disclose or suggest selecting *nm*-bit data (where $nm \geq 8$, as $n \geq 2$ and $m \geq 4$) by *y*-bits (where *y* is less than *nm* but greater than 1) for sequential output to *y* output pads (where *y* is less than *nm* but greater than 1).

In particular, Kim does not disclose or suggest selecting the 8-bit data disclosed therein by less than 8-bits but more than 1-bit for sequential output to less than 8 but more than 1 output pad. Rather, as noted above, all 8 bits of error data error<0:7> of Kim are

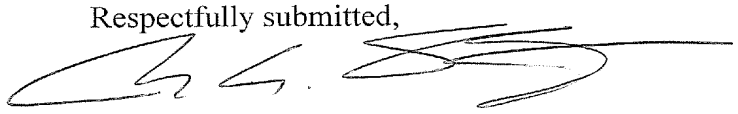
serialized and output via the shift register **301** to one test pad DQB0. *See* Kim, Col. 6, lines 8-13. Indeed, as further noted in Kim, "during a DA mode test, DQB1, DQB2, and DQB3 have no test output." Kim, Col. 6, lines 24-25. Thus, Kim fails to disclose or suggest at least the "selecting" and "outputting" recitations of Claim 1. Nor does the AAPA disclose or suggest these recitations, as noted in the Final Action. *See* Final Action, Page 4.

Accordingly, Applicants submit that neither the AAPA nor Kim discloses or suggests at least "outputting y-bit comparison result data selected by selecting, by y bits generated from the first memory cell array or from the second memory cell array, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively," as recited by amended Claim 1. Thus, Applicants submit that amended Claim 1 is patentable over the combination of the AAPA and Kim for at least these reasons. Amended Claim 11 includes similar recitations, and is thus patentable for at least similar reasons. Amended Claims 10 and 21 similarly recite grouping and outputting "the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal," and are likewise patentable for at least similar reasons. Also, dependent Claims 2, 3, 12, 13, and 37-41 are patentable at least per the patentability of Claims 1, 10, 11, and 21 from which they depend.

Conclusion

Based on the remarks provided above, Applicants respectfully submit that all of the pending claims are now in condition for allowance. Thus, Applicants respectfully request withdrawal of the outstanding rejections, allowance of the pending claims, and passing the application to issue. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,



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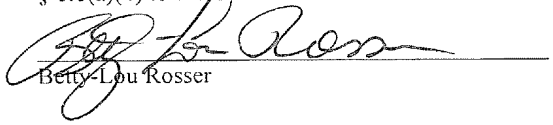

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